REMARKS

The Examiner is thanked for the due consideration given the application.

Claims 1-7 and 9-20 are pending in the application. Claims 9 and 13 have been amended to adjust their dependencies.

No new matter is believed to be added to the application by this amendment.

Claim Objections

Claims 9 and 13 have been objected to as containing informalities. Claims 9 and 13 have been amended to be free from informalities.

Rejections Under 35 USC §103(a)

Claims 1-5, 7-11 and 16-19 have been rejected under USC §103(a) as being unpatentable over ROLSTON et al. (U.S. Publication 2002/00331199) in view of CEDRONE et al. (U.S. Patent 6,538,987). Claim 6 has been rejected USC §103(a) as being unpatentable over ROLSTON et al. in view of CEDRONE et al., and further in view of PULESTON (U.S. Publication 2002/0181480). Claims 12, 13 and 20 have been rejected USC §103(a) as being unpatentable over ROLSTON et al. in view of CEDRONE et al., and further in view of SEKI et al. (U.S. Publication 2004/0213247).

These rejections are respectfully traversed.

The present invention pertains to an ATM system having alternative switching in case of clock failure. The present

invention is illustrated, by way of example, in Figure 1 of the application, which is reproduced below.

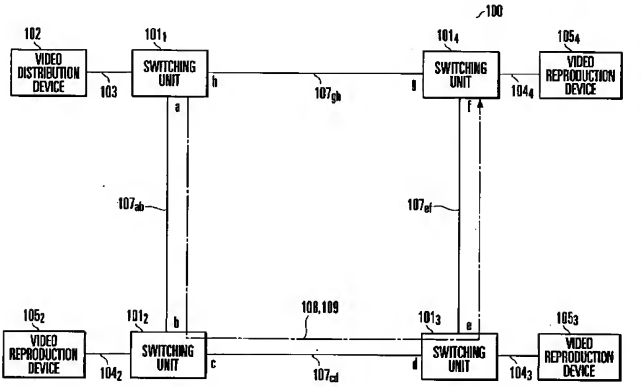

FIG. 1

Figure 1 shows a loop configuration of switching units, which allows alternative switching routes for clock signals. Claim 1 of the present invention sets forth: "at least one relay node which is positioned in a clock supply route formed by coupling arbitrary virtual paths for a loop of nodes in a network." Claim 1 of the present invention also sets forth first and second port switching means where "the first and second port switching means forming upstream and downstream switching ports."

ROLSTON et al. pertain to distributed synchronous clocking. The Official Action refers to Figure 1 of ROLSTON et al., which is reproduced below.

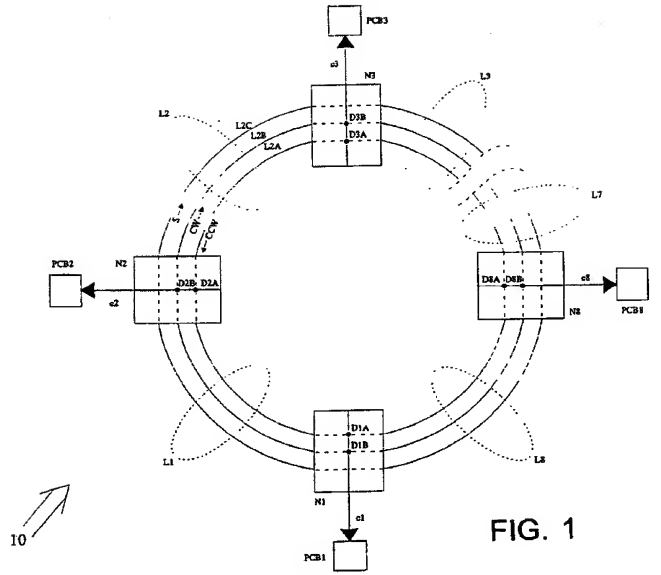

FIG. 1

Figure 1 of ROLSTON et al. shows a synchronous clocking system having nodes N1 . . . N8 connected by propagation channels L1 . . .L8. N1 is a masternode. Paragraph 0040 of ROLSTON states:

> Synchronization of the clock signals c1, c2, c3, . . . , c8, is achieved by propagating two trains of pulses CW and CCW around the nodes N1, N2, N3, . . . N8 in opposite directions. The pulse trains CW and CCW are generated in master node N1, which transmits them to the slave nodes N2, N3, . . . N8, by way of propagation channels provided by transmission links L1, L2, L3, . . . L8 which interconnect the nodes N1, N2, N3, . . . N8 to form a ring. The transmission links L1, L2, L3, . . . L8 actually comprises three parallel propagation paths. The two innermost paths, designated A and B carry the pulse trains CW and CCW, respectively, and the third path, designated C, carries a slower pulse train S. Although each of the

> transmission links L1, L2, L3, . . . L8 is shown as if it comprised three distinct wires, in practice, it would preferably comprise a single transmission medium so that all three trains of pulses would experience the same propagation delay.

By this, ROLSTON et al. teach that the transmission links L1 . . .L8 are set paths. In contrast, the present invention sets virtual paths where claim 1 sets forth: "at least one relay node which is positioned in a clock supply route formed by coupling arbitrary virtual paths for a loop of nodes in a network." On the other hand, the "hard wired" technology of ROLSTON et al. is unable to set "arbitrary virtual paths."

Also, paragraph 0039 of ROLSTON et al. teaches that 8 or more nodes are used. In contrast, the present invention's selection of arbitrary virtual paths result in as few as 4 nodes being used, as is set forth in claims 10 and 11.

The Official Action acknowledges that ROLSTON et al. fail to teach fault detection means, fault notification transmission means, sending fault notification data, first port switching means, a switching port, a termination node having second port switching means, performing port switching, first and second port switching means forming upstream and downstream switching ports, and port switching instruction means. The Official Action refers to CEDRONE et al. for these teachings.

CEDRONE et al. pertain to a rapid ring protection switching system where primary and secondary virtual circuits are

set up over primary and secondary routes (Abstract). The Official Action typically refers to column 3, lines 36-38 of CEDRONE et al., which states: "A system employing the inventive rapid ring protection switching sets up corresponding virtual circuits over both the selected ring and the non-selected ring." The Official Action also cites other portions of CEDRONE et al. for additional teachings related to the virtual circuits.

However, the primary reference of ROLSTON et al. does not use virtual circuits but rather uses multiple hard-wired channels. There is thus no reason to utilize virtual circuits in the technology of ROLSTON et al. Applying the technology of CEDRONE et al. thus changes the principle of operation of ROLSTON et al.

If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).

One of ordinary skill and creativity would thus fail to produce a claimed embodiment of the present invention from a knowledge of ROLSTON et al. and CEDRONE et al. The other applied references of PULESTON and SEKI et al. fail to address the deficiencies of ROLSTON et al. and CEDRONE et al. A *prima facie* case of unpatentability has thus not been made.

These rejections are believed to be overcome, and withdrawal thereof is respectfully requested.

Conclusion

The Examiner is thanked for considering the Information Disclosure Statement filed January 5, 2004 and for making an initialed PTO-1449 Form of record in the application.

Prior art of record but not utilized is believed to be non-pertinent to the instant claims.

The Examiner's rejections are believed to have been overcome, obviated or rendered moot and that no issues remain. The Examiner is accordingly respectfully requested to place the application in condition for allowance and to issue a Notice of Allowability.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

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